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Description

Forming Collar Structures in Deep Trench Capacitors With Thermally Stable Filler Material

Background of Invention

[0001] The field of the invention is that of forming DRAM cells having high aspect ratio trenches in integrated circuit processing.

[0002] As ground rule dimensions shrink in integrated circuits, the problem of filling high aspect ratio trenches increases, in particular for trench capacitors used in DRAM cells that are commonly used in advanced processing.

[0003] The industry-standard filling process has been photoresist, applied and stripped several times. This method has been widely adopted because photoresist is well understood.

[0004] Since resist cannot stand the high temperatures used in front end processing, it is necessary to strip the resist and refill the trench when a step is to be performed at a tem-

perature greater than 300C. This occurs more than once in the course of the deep trench processing module.

[0005] As an additional consideration, the lengthy processes required to fabricate an integrated circuit are currently highly integrated; i.e. a change in a single process step can affect the result of steps performed before and after it, sometimes affecting steps that are not immediately before or after, but separated in time by several other steps.

[0006] It is therefore a multi-dimensional or multi-factor decision to change a process step. It is not enough that the new step produce a tougher, or thinner, or lower-density film, or take less time to put down. It is also required that the new step not produce disadvantages in other aspects of the process that outweigh the benefits.

[0007] The steps in a typical prior art method up to forming the buried plate of the trench capacitor are a) etching a deep trench in a silicon substrate; b) forming a barrier layer on a trench sidewall; c) filling the trench with photoresist; d) recessing (etching) the photoresist to a predetermined depth, so a top part of deep trench is exposed; e) removing the barrier layer in the upper region to expose the trench sidewall; f) stripping the photoresist; g) forming a collar on the side wall upper portion using the barrier

layer as a mask in the lower portion; and h) forming a buried plate diffusion region in the trench lower region using the collar as a mask for the upper portion.

[0008] The main function of the barrier material in the prior art method is to protect the lower portion of the trench during the steps of forming the collar.

[0009] The barrier material is typically nitride or a composite of oxide and nitride.

[0010] This is a fairly complicated and expensive process and it would be highly desirable to have a process with fewer and/or less expensive steps that produced an equivalent result.

[0011] In a particular prior art example, shown in US Patent 6271142, the method uses a partial fill scheme of deep trenches with spin-on material that is immediately followed by a collar formation. Partial fill of deep trenches has a very high non-uniformity of SOG (the reference point is thickness of SOG material at deep trench bottom - thousands of Angstroms). This approach can not be implemented in manufacturing. Partial fill requires an ideal structure with all Deep Trenches being of identical size since SOG thickness is proportional to trench volume. This method can not fill trenches of different sizes and vol-

umes, which is typical for any real DRAM device. The patent also does not address the problem of final removal of SOG from the wafer surface, since it does not use any etch or CMP techniques.

[0012] SOG has a tendency to outgas and/or to crack or delaminate as a result of thermal stress. The probability of cracking is dependent on the thickness of the layer and also on the density of the pattern and topology. Those skilled in the art have been reluctant to use SOG as a trench filler because of the cracking problem and the difficulty of predicting what thickness is safe to use.

Summary of Invention

[0013] The invention relates to a simplified process for forming a deep trench capacitor up to the formation of the buried plate that eliminates the deposition and removal of the barrier material.

[0014] A feature of the invention is the use of a Low cost, temperature stable spin-on material as a sacrificial material instead of photoresist.

[0015] Another feature of the invention is the elimination of some steps in the creation of a collar structure on a deep trench sidewall.

[0016] Another feature of the invention is the use of atomic layer

deposition (ALD) for collar deposition.

[0017] ALD has an advantage of producing high quality materials (such as SiN and SiO2) at a relatively low temperature range (250-650C). The benefits of lowering the temperature budget of deposition are described in detail below.

[0018] The process comprises the following basic steps:

[0019] a) formation of a deep trench in a silicon substrate; filling the trench with temperature stable spin-on material;

[0020] Optional anneal of spin-on material to higher temperature is recommended preferably matching the temperature of subsequent collar deposition;

[0021] b) Recess (etch) the spin-on material to a pre-determined depth so the top part of deep trench is exposed;

[0022] As an alternative chemical mechanical polish (CMP)of spin-on material could be used if necessary before recess to improve recess uniformity;

[0023] c)Form a collar on deep trench sidewall upper portion;

[0024] d)Remove the spin-on material from trench bottom by a wet etch; and

[0025] e)Form a buried plate in the trench lower region.

[0026] As described above, an essential consideration of the decision to introduce a new process is whether its advan-

tages, e.g. lower cost, outweigh its disadvantages.

[0027] While additional SOG anneal and CMP steps could add to process cost, these steps are typically are less expensive than resist reactive ion etching (RIE) steps. Cost of spin-on material is also typically much less than CVD type of materials. The greater advantage of the proposed scheme in its flexibility, since its eliminating temperature budget restrictions of resist based schemes.

[0028] The spin-on material has a molecular weight of between 1,000 and 10,000. It is applied as dissolved in a solvent for the spin-on step. The solvent is driven off in a pre-bake step at relatively low temperature (less than about 350degC) and the material is cured by heating in various ambients.

[0029] The identified temperature stable spin-on material is poly-silazane, which has excellent gap filling properties and was shown to fill deep trenches with aspect ratio of 40-60. The material has a structural formula of [SiNR1R2NR3]n, where R1, R2 and R3 are all hydrogen in the case of inorganic poly-silazane and are alkyl, aryl, or alkoxyl organic radicals in organic poly-silazane. For convenience, the term poly-silazane will be shortened to silazane.

Brief Description of Drawings

[0030] Figure 1 illustrates a section of a silicon wafer after preliminary steps in the formation of a trench capacitor.

[0031] Figure 2 illustrates the same section after depositing a liner according to the invention.

[0032] Figure 3 illustrates the same section after stripping the temporary filler in the lower portion of the trench.

[0033] Figure 4 illustrates the same section after widening the lower portion of the trench.

[0034] Figure 5 illustrates the same section after deposition of an alternative collar material.

[0035] Figures 6A and 6B illustrate a potential parasitic transistor.

[0036] Figure 7 illustrates a C-V curve shown the improvement in Vt provided by the alternative material.

Detailed Description

[0037] Figure 1 illustrates a portion of a silicon wafer after a number of preliminary steps including forming pad oxide 20, pad nitride 30, forming a deep trench (nominally about 8 microns deep and having an aspect ratio of greater than 40) in a conventional reactive ion etch step, filling the trench with a temporary filler material, illustra-

tively spin-on glass (SOG) and recessing the SOG to provide room for forming a dielectric collar. A conventional planarizing step, e.g. by chemical-mechanical polishing, may be performed at any convenient time.

[0038] An anneal step is performed after filling the trenches with SOG (or after SOG CMP). For polysilazane, an oxidizing anneal ambient is preferred. Preferably, the temperature of the anneal is relatively close to the temperature of collar material deposition in order to prevent excessive SOG outgassing during deposition. Such an anneal/cure can be done in-situ in the spin-on track (the tool used for spin-on application) during the spin-on application if the deposition has a low temperature budget of less than 500C (such as ALD).

[0039] Figure 2 shows the result of forming a spacer 120 as discussed below. According to the invention, a nitride layer is deposited using atomic layer deposition (ALD), which is performed at low temperature, e.g. 250 - 650 C.

[0040] The low temperature deposition is an advantage, because SOG has a tendency to outgas and/or to crack or delaminate as a result of thermal stress. The probability of cracking is dependent on the thickness of the layer and also on the density of the pattern and topology. Those

skilled in the art have been reluctant to use SOG as a trench filler because of the cracking problem and the difficulty of predicting what thickness is safe to use. Also, since the wet etch rate of polysilazane based spin-on material decreases with an increase in anneal temperature, it becomes important to keep the temperature budget of SOG as low as possible. SOG annealed at lower temperature (< 650C)is much easier to remove from the trench bottom than SOG annealed at a temperature greater than about 700C. Therefore, low temperature ALD deposition of collar material can provide a pathway for further improvement in process time and throughput due to significantly reduced SOG etch removal times.

[0041] With an ALD deposition according to the invention, the amount of outgassing, probability of cracking or delamination and SOG etch times are much reduced.

[0042] After the spacer material has been put down and the material on the bottom of the aperture 150 has been etched to form the spacer itself, the SOG material is removed, e.g. in a wet etch process, as shown in fig 3, leaving the entire depth of the trench ready for doping the buried plate, e.g. by gas phase doping, depositing the node dielectric and filling the trench with the center electrode to

complete the capacitor.

[0043] In another aspect of the invention, a conventional process of depositing low pressure nitride may be used for the spacers, as shown in Figure 5. In that case, the SOG is a thermally stable material, e.g. polysilazane, that is cured at a temperature of less than 450C and then annealed, either in an oxygen ambient or in an ambient containing water vapor, at a relatively high temperature of 700 - 1200 C. Inert ambient anneal typically produces high tensile stress in SOG and could cause cracking. With annealing, the SOG can withstand the deposition temperature of LP nitride (600-800C), which provides a considerable advantage and process simplification over the prior art of a resist fill. The Figure shows the result after stripping the temporary filler material, leaving the aperture 160 (in this case having been extended in a bottle etch step), with a capacitor dielectric 45 and sidewalls 125.

[0044] In another aspect of the invention, the collar is made of a high-k material, meaning Al2O3, HfO2, ZrO2 and La2O3 and their silicides; and the like. The preferred deposition method for these materials is also ALD, with its low temperature. The low temperature deposition process is considered advantageous, since it exerts less thermal stress

in SOG.

[0045] Figure 6A shows an overall view of a trench after a "bottle etch" step of widening the aperture that will hold the capacitor and showing in detail 5 the location of a possible parasitic FET. In Figure 6B, dotted oval 130 encloses the vertical cell transistor, with gate 135, gate dielectric 133, body 134, and lower electrode 132. The dotted oval 127 encloses an area extending from the buried plate 40 of the capacitor to the buried strap 132 of the vertical transistor 130. When the voltage on the center electrode 165 of the capacitor is high, there is a potential for the formation of a parasitic transistor, with electrode 165 as the gate, collar 125 as the gate dielectric, buried plate 40 as one electrode and buried strap 132 as the other electrode.

[0046] The high-k dielectrics, in particular AL2O3, also have the advantage that they trap a large quantity of fixed negative charge and therefore raise the threshold of forming parasitic vertical transistors in the substrate, with the buried plate as one electrode and the buried strap as the other.

[0047] Figure 7 shows a C-V curve with the results of a parasitic transistor based on a conventional oxide collar in curve 172 and a high-k collar (Al2O3) in curve 170. The high-k curve has shifted to the right, indicating a higher thresh-

old (by 0.6V) for the formation of parasitic transistors.

[0048] An optional feature of the invention is the use of a bottle etch step before the collar formation step.

[0049] Another optional feature of the invention is the use of an ALD collar put down as a preliminary step in forming a high-k collar.

[0050] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.